VCO LINEARISATION BY FREQUENCY FEEDBACK

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ABSTRACT

We demonstrate, how a voltage controlled oscillator is linearised by frequency feedback independently of the VCO-characteristic. The VCO is replaced by a controlled frequency locked loop. Hereby, the VCO characteristic is substituted by the inverse function of the frequency detector characteristic, which, in our case, is linear to a great extent. A 70 MHz oscillator was built to verify the principle.

INTRODUCTION

Electrically tunable oscillators are an important subsystem in carrier recovery loops and frequency synthezisers. They are most frequently tuned by voltage sensitive capacitive diodes known as varactor diodes [1]. Due to the characterisitic of the diode and the tank circuit, the VCO gain is quite nonlinear. The modulation sensitivity can easily vary by 10:1 over a useable tuning range [2]. For most applications a linear characteristic is preferable.
In phase locked loops (PLL's), for instance, the nonlinearity leads to a variation in the bandwidth of the PLL. This can cause an excessive lock-in time or even instability. The effect is particularly severe in frequency synthesizers, that have to manage large frequency steps.

LINEARISED VCO

Frequency Locked Loop

To obtain a linearisation, the VCO is substituted by a frequency locked loop (FLL). Normally, the aim of a FLL is to lock a tunable oscillator onto a reference [4]. In this application the reference oscillator can be avoided. The FLL consists, therefore, only of a VCO, frequency discriminator (FD), and control filter (CF). The general structure is shown in figure 1, where a summing node was inserted behind the FD.

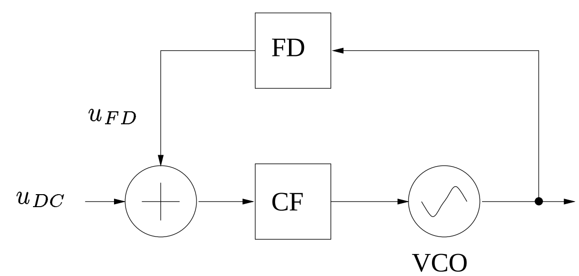

Figure 1: Frequency locked loop

The frequency discriminator compares the frequency of the VCO with a reference. For the case of a delay line discriminator, the delay line furnishes the frequency reference. The sum of the error signal u_{FD} and the offset voltage u_{DC} is fed back to the VCO by a control filter. The error signal u_{FD} has to compensate the offset created by u_{DC}. Thus, the error signal is not zero. The VCO frequency is shifted with respect to the reference frequency, dependent on the volt-

age u_{DC}. Hence, the structure can be used as a new VCO, where u_{DC} is the control voltage and ω_{VCO} is the output frequency.
It is commonplace to use a simple integrator as the loop filter for frequency tracking loops [3]. In this case, the system can be described by the following nonlinear differential equation:

$$\frac{d\omega_{VCO}}{dt} = \frac{k_O}{T}\left(u_{DC} + g(\omega_{ref} - \omega_{VCO})\right) \quad (1)$$

where ω_{VCO} is the frequency of the VCO, ω_{ref} the reference frequency in the discriminator, $g(\omega)$ the odd and nonlinear frequency discriminator characteristic, k_O the VCO sensitivity, and T the integrator constant.
In the steady-state, the derivative with respect to time of the VCO frequency is zero and thus

$$\lim_{t\to\infty} \omega_{VCO} = \omega_{ref} + g^{-1}(u_{DC}) \quad (2)$$

The characteristic of this new VCO is given by the inverse function of the frequency discriminator characterisitic. The new characterisitic is independent of the VCO sensitivity k_O. A variation of k_O has no effect on the new sensitivity.
The quiescent frequency of the new VCO is equal to the reference frequency in the discriminator and does not depend on the tank circuit in the oscillator.
Due to the behavior of the frequency locked loop the control voltage u_{DC} of the new VCO is additionally filtered by the closed-loop transfer function of the FLL. In the case of an ideal integrator as a control filter, the transfer function is a simple, one-pole low-pass filter.

$$H_{FLL} = \frac{\omega_{FLL}}{s + \omega_{FLL}} \quad (3)$$

with

$$\omega_{FLL} = \frac{k_O\, k_{FD}}{T} \quad (4)$$

where k_{FD} is the frequency discriminator sensitivity.

Frequency Discriminator

A delay line discriminator is used as a frequency detector. This kind of detector is well known for phase noise measurements. A detailed description can be found in [5]. The block diagram of this kind of discriminator is shown in figure 2.

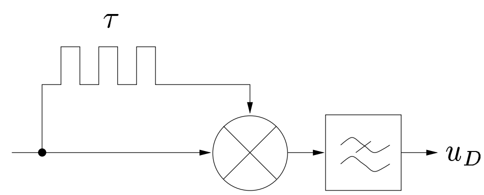

Figure 2: Delay line discriminator

If the incoming signal is sinusoidal with frequency ω_{in}, the detector ouput signal u_D is

$$u_D = k_m \cos(\omega_{in}\tau) \quad (5)$$

where k_m is a constant, which includes the signal amplitude and the multiplier constant. For

$$\tau = (2n+1)\frac{\pi}{2\omega_{ref}} \quad (6)$$

the output signal is

$$u_D = (-1)^n k_m \sin(\Delta\omega\,\tau) \quad (7)$$

where $\Delta\omega = \omega_{in} - \omega_{ref}$. The delay line discriminator converts a frequency offset into a phase offset with the delay line, which is then detected with an analog multiplier or a mixer as a phase detector. The sinusoidal characteristic of the phase detector is due to the sinusoidal input signal. For the case of a rectangular input signal, the characteristic is given by

$$u_D = (-1)^n k_m \arcsin\left(\sin(\Delta\omega\,\tau)\right) \quad (8)$$

The new characteristic is a triangular function and piecewise linear. Figure 3 shows the new characteristic.

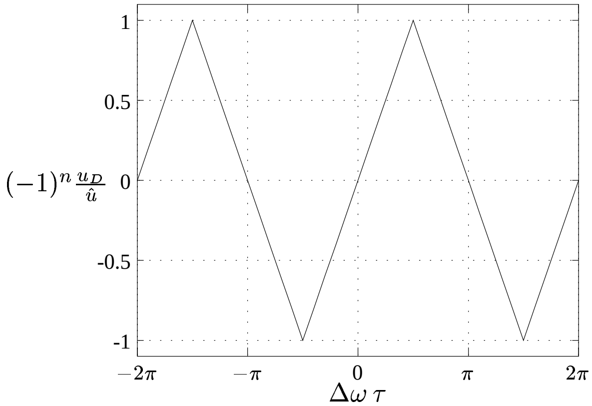

Figure 3: Frequency detector characteristic

Other phase detectors may be used, e. g. an exclusive-or gate, which is easier to implement. The modified structure is shown in figure 4, where an additional amplifier was incorporated behind the frequency discriminator to adjust the gain.

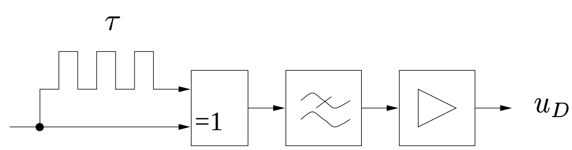

Figure 4: Modified delay line discriminator

To avoid the possibility of false-locking due to multiple zero-crossings of the frequency detector characteristic, the VCO range and the delay have to be chosen properly. The VCO offset from the reference must be smaller than $2\omega_{ref}/(2n+1)$ at start up and the maximum possible offset from ω_{ref} for the new VCO is $\omega_{ref}/(2n+1)$.
Due to the discriminator transfer response, the detector output signal is filtered by the function

$$H_{FD} = \frac{\sin(\omega\frac{\tau}{2})}{\omega\frac{\tau}{2}} \qquad (9)$$

However, this effect can be neglected as long as the bandwidth of the FLL is far smaller than $1/\tau$.

EXAMPLE

A voltage controlled oscillator at 70 MHz was built to verify the theory. Fig. 5 shows the measured VCO characteristic for the free-running VCO and the FLL, which serves as a VCO.

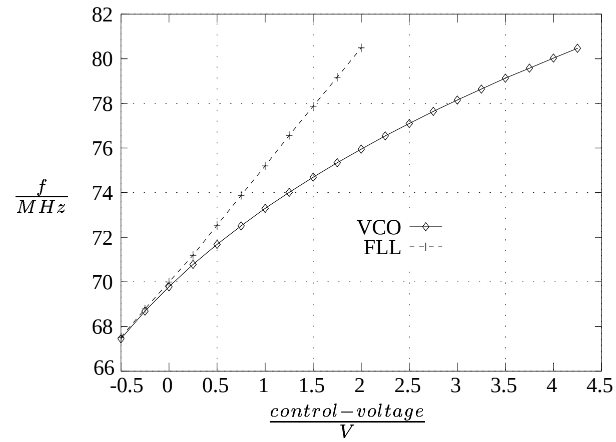

Figure 5: VCO characteristic (measured)

The delay in the frequency discriminator was about 3.57 ns and the bandwidth of the FLL was 1 kHz.
As expected, a highly linear characteristic can be observed for the FLL because of the piecewise linear frequency detector characteristic.

INCORPORATION INTO A PLL

For applications in phase locked loops the additional lowpass H_{FLL} increases the order of the PLL by 1. The bandwidth ω_{FLL} of the lowpass filter depends on the VCO gain k_O. The nonlinearity of the VCO causes now a variation in the bandwidth.
The minimum bandwidth of the FLL has to be chosen carefully. The additional poles have to be far away from the dominant poles, so that the behavior of the PLL is not influenced significantly. The lowpass may also be considered as a part of the control filter.

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CONCLUSION

It has been shown that the characteristic of a voltage controlled oscillator can be linearised, if the VCO is incorporated into a frequency locked loop and a delay line discriminator is used as a frequency detector. The shown structure has moreover the advantage that the quiescent frequency of this new VCO is given by the delay line in the discriminator. The quiescent frequency is independent of the thermal drift and aging of the oscillator. Hence, we also expect a better long-term stability.

We assume, furthermore, that the structure can also be used to reduce the oscillator phase noise, if the noise floor behind the frequency detector is lower than the detected frequency noise. However, this effect could not be observed in the realized structure due to the fact that we used a frequency detector with a very low sensitivity.

All additional elements apart from the delay line can be easily incorporated in an integrated circuit.

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